Self-Heating Effects on the Thermal Noise of Deep Sub-Micron FD-SOI MOSFETs

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***Abstract*—Self-heating effects became more prominent with the introduction of the modern devices like FD-SOI and low thermal conductivity materials such as SiO_2. Consequently, the temperature rise of a device due to its self-heating is pronounced more as the gate lengths shrink and the power density values increase. In analog design, one of the main drawbacks of elevated temperature is the deterioration of the thermal noise performance. For observing the thermal noise performance of FD-SOI MOSFETs, a thermal model for the device self-heating is used. The influence of self-heating on the thermal noise is examined by activating and inactivating the self-heating thermal model and comparing the results. It is shown that self-heating can deteriorate the thermal noise current (up to 18%) and the input referred thermal noise voltage (up to 37%) significantly for short channel FD-SOI devices.**

***Keywords*—Self-heating, FD-SOI, thermal noise, thermal modelling**

I. Introduction

One of the main drawbacks of device scaling is the increased power density and the resulting elevated temperature. Operation at high temperature has many drawbacks like leakage, lower mobility, electro-migration and so on [1]. One of the main drawbacks is the increased device thermal noise in analog design since thermal noise has a direct relation with the absolute local temperature of the device. Especially after the introduction of the modern MOSFET device geometries like Fully Depleted Silicon on Insulator (FD-SOI), self-heating became a more critical problem [2]. This is mainly due to the low thermal conductivity materials like $\mathrm{SiO_2}$ which are necessary for the implementation of FD-SOI devices [3]–[5]. In these devices, low thermal conductivity barriers surround the channel, in which the power is mostly dissipated. Consequently, the generated heat in FD-SOI MOSFETs cannot find a low-resistance path for diffusing outside the device borders. The generated heat turns into elevated temperature in nanometer scale local spots, which are comparable to the dimensions of transistors in FD-SOI. The device temperature becomes even higher when compared to the average temperature of the chip, which is already much larger than the room temperature due to the high-density power dissipation of the other neighbour devices. Therefore, it is necessary to take into account the temperature rise due to the self-heating of the device while designing a block where low noise operation is critical.

This work is intended to analyse the thermal noise of a device considering its self-heating and show the influence of self-heating on its thermal noise performance. For that, a self-heating thermal model is used for activating and inactivating the self-heating effects and observing the significance of the elevated temperature due to device self-heating. The thermal model for the self-heating is included in the device model by the design kit, which is a commercially available 28nm FD-SOI technology.

In Section II, the theory of thermal noise in MOSFET devices is given in addition to different short channel thermal noise models proposed by different authors. In Section III, thermal noise current and input referred thermal noise voltage performance of FD-SOI MOSFET devices are compared for the cases where self-heating is activated and inactivated. Finally, in Section IV, the summary of the work and the conclusions are provided.

II. Theoretical Background and Related Work

The power spectral density of the thermal noise current in the channel of a MOSFET device is given by [6]

$$S_i = 4kT\gamma g_{d0} \tag{1}$$

where k is the Boltzmann constant, T is the absolute temperature, g_{d0} is the zero-bias drain conductance of the MOSFET device (i.e. the drain conductance of the device when $\mathrm{V_{DS}} = 0\mathrm{V}$ is applied) and γ is the excess noise coefficient. For long channel devices in strong inversion, γ takes values between 1 and 2/3 while moving from linear region to saturation. However, for devices with a short channel, the value of γ tends to be larger due do various factors. *Channel length modulation* is one of the effects that increase γ for short channel devices. Increasing $\mathrm{V_{DS}}$ creates a pinch-off region on the drain end and decreases the effective length of the device where the inversion layer charge is present in the channel. This would increase the thermal noise current as the device moves deeper into saturation [7]. *Velocity saturation* is another factor that affect the charge density and consequently the thermal noise current of the device. In [8]–[10] the authors included velocity saturation in the derivation of the thermal noise current and observations made on an increasing trend of γ under smaller channel lengths and higher velocity saturation.

Most of the authors explain the large γ by *hot electron effect* [8], [10]–[12]. This effect is mainly observed in short channels under large $\mathrm{V_{DS}}$ voltage. Large lateral electric field in the

channel creates hot electrons which have higher temperature (i.e. larger average kinetic energy) when compared to the lattice temperature. In that case, the average temperature of these hot electrons has to be considered rather than the lattice temperature. The temperature of the hot electrons can be approximated by [13]

$$T_e = T_L \left(1 + \frac{E}{E_c}\right)^n \tag{2}$$

where T_e is the hot electron temperature, T_L is the lattice temperature, E_c is the critical electric field and E is the lateral electric field in the channel with n = 2, 1, or 0. While n = 0 corresponds to no hot carriers case, n = 2 gives the other extreme. In [10], (2) is modified as $T_e = T_L + \delta T_L \left(\frac{E}{E_c}\right)^2$ where δ is used as a fitting parameter to adjust the simulations to the measurement. With the hot carrier model, the higher temperature electrons show more random fluctuations and this can be modelled by providing a larger γ in (1).

Another explanation of larger γ under very large V_{DS} is the *avalanche multiplication* [11], [14]. When V_{DS} is larger than the band-gap voltage, high energy carriers are scattered by valence band electrons and additional electron-hole pairs are created. The thermal fluctuations of these additional carriers contribute to the overall noise and this increases γ.

The listed modifications on the thermal noise current provide good approximations for the short channel devices; however, they don't account for the self-heating of individual devices *for a large range of bias conditions* or they assume the increase in γ due to self-heating is already included in the model by fitting between measurements and simulations. For obtaining more realistic values for the power spectral density of thermal noise current under different bias conditions, one has to estimate the individual temperature of a device accounting its self-heating effects. Most of the current simulators can find solutions under a single temperature input that is valid for all the devices in the net-list. Consequently, different devices with different lattice temperatures are assumed to have the same temperature value. This would result in some errors in the calculation of the thermal noise current and hence in the noise figure of amplifiers, especially when they are implemented in advanced technologies like FD-SOI, FinFET where the devices are confined inside low thermal conductance materials. As it has been already mentioned, very large temperature gradients and different temperature values in short distances can be observed in these technologies, mainly due to low thermal conductance and high power densities [2]–[5]. Therefore, the noise analysis should be performed simultaneously by considering the self-heating effects.

III. Thermal Noise Considering Self-Heating

A. Thermal Model for Self-Heating

The temperature rise of each device due to their individual self-heating is calculated by considering the thermal model of Fig. 1. According to the model, R_{th} is the thermal resistance and C_{th} is the heat capacitance. The values of these

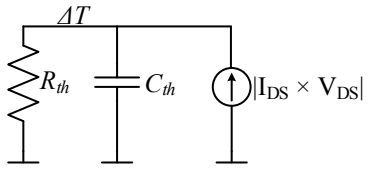

Fig. 1: The thermal model that provides the temperature rise of each device due to their self-heating [15].

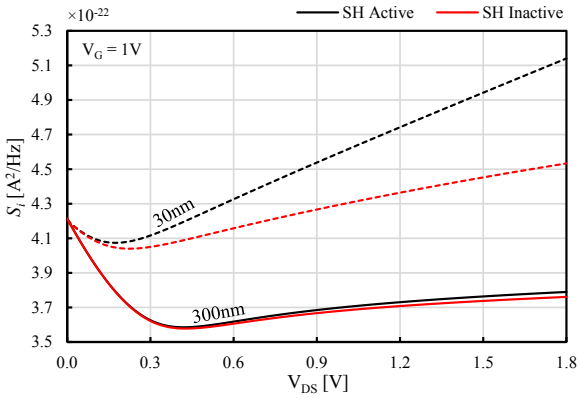

Fig. 2: Thermal noise current (S_i) of 30nm and 300nm nMOS devices for the cases where self-heating thermal model is active and inactive.

parameters are calculated for each device according to their geometries (width, length, number of fingers etc.) The power dissipation of the device is modelled by a current source. The temperature value on the upper common node gives the temperature increase ΔT of the device due to its self-heating. The complete model is included in the device by the design kit provider and can be switched on or off for a specific simulation. Consequently, with the provided self-heating model, it is possible to consider the self-heating effects for all bias conditions.

B. Thermal Noise Current

For observing the effect of self-heating on the thermal noise current, nMOS devices with different gate lengths are simulated by activating and inactivating the self-heating thermal model. The gate lengths of the devices are varied from 30nm to 300nm. The gate voltage is kept constant and V_{DS} is set as the sweep parameter. All devices are implemented with 20 fingers and their finger width is adjusted so that their zero bias drain conductance is set approximately equal to 20mA/V. Like that, all devices have equal thermal noise current under no power dissipation and no self-heating. Fig. 2 shows the thermal noise current. The relatively large thermal noise current in the 0 - 300mV window is due to linear region operation. The increase in the noise with V_{DS} in the saturation can be explained with velocity saturation and hot electrons. In addition to these observations, it can be seen that for the short channel device (L = 30nm), thermal noise current shows quite different trends for the cases where self-heating is activated and inactivated. For low V_{DS} values, the two curves are almost overlapping. On the other hand, as V_{DS} increases, the curves start to split. This is because of the higher power dissipation under larger V_{DS} and the consequent higher operating temperature due to

TABLE I: Parameters for the devices with the gate lengths of 30nm and 300nm.

Parameter	L	W	Power	$g_m\|_{V_{DS}=1V}$	g_{d0}
Unit	nm	nm	mW	mA/V	mA/V
Short Channel	30	20 × 305	6.25	9.14	20.01
Long Channel	300	20 × 1068	5.86	17.66	20.00

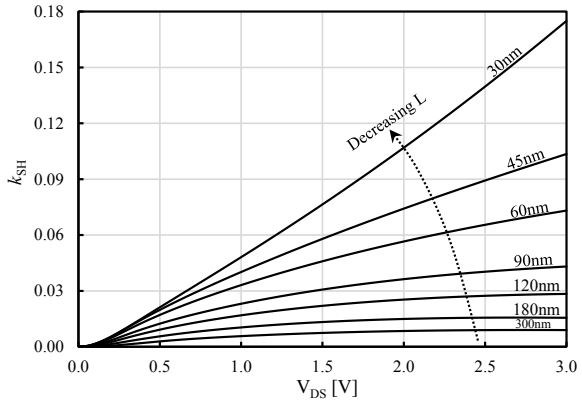

Fig. 3: Self-heating error factor (k_{SH}) with respect to V_{DS} for devices with different gate lengths from 30nm to 300nm.

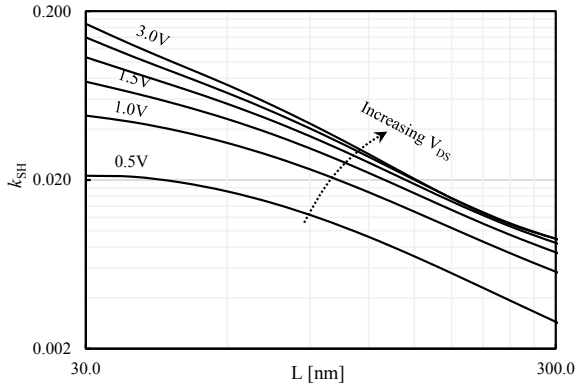

Fig. 4: Self-heating error factor (k_{SH}) with respect to gate length for V_{DS} = 0.5V, 1.0V, 1.5V, 2.0V, 2.5V, 3.0V. For V_{DS} = 0V, k_{SH}=0.

self-heating. The same observation can also be made for the long channel device (L = 300nm); however, the difference is much less significant than the short channel device. This is not due to the lower power dissipation of the long channel device when compared to the short channel one. In fact, their power dissipation values are more or less the same (Table I); however, the short channel device has a much smaller area and its resulting power density is much larger. Therefore, the temperature of the short channel device rises to a much higher value due to its self-heating and that results in a large thermal noise current. For observing the effect of self-heating on the thermal noise current, we can define the self-heating error factor k_{SH} as

$$k_{\mathrm{SH}} = \frac{S_{i,\mathrm{SH}} \quad S_i}{S_i} \tag{3}$$

where $S_{i,\mathrm{SH}}$ is the thermal noise current (black curves on Fig. 2) when self-heating is considered and k_{SH} is the self-heating

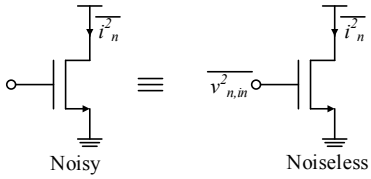

Fig. 5: Model of the noisy device with a fictitious input referred noise voltage source $\overline{v^2_{n,in}}$

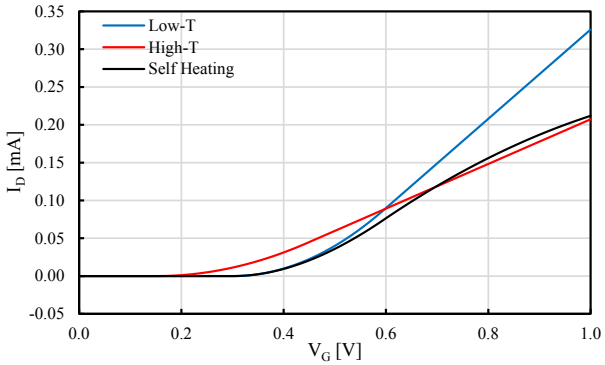

Fig. 6: V_G-I_D curves for low temperature, high temperature and activated self-heating. The curves are for illustration of the behaviour of g_m under different thermal conditions.

error factor. Therefore, by combining (1) and (3) $S_{i,\mathrm{SH}}$ can be written as

$$S_{i,\mathrm{SH}} = 4kT\left(1 + k_{\mathrm{SH}}\right)\gamma g_{d0} = \left(1 + k_{\mathrm{SH}}\right)S_i. \tag{4}$$

Fig. 3 and Fig. 4 show the amount of error when self-heating is not taken into account. The error becomes larger linearly with increasing V_{DS} and exponentially with decreasing gate length. Moreover, the error can go up to 18% under very large V_{DS} for 30nm gate length.

C. Input Referred Thermal Noise Voltage

In many applications like LNA design, the figure of merit for noise performance is the voltage quantity instead of the current since a voltage level is sensed at the output of the previous stage rather than the current. Hence, the performance of blocks are measured by parameters like input referred noise voltage or noise figure. Therefore, one should consider the self-heating effects also on the other parameters that influence the input referred noise voltage. The input referred noise voltage (Fig. 5) of a device can be expressed as (Fig. 5)

$$S_{v,in} = \frac{S_i}{g_m^2} = \frac{4kT\gamma g_{d0}}{g_m^2} \tag{5}$$

where g_m is the gate-to-drain transconductance of the device. In (5), g_{d0} is not influenced by the self-heating since the parameter is set at the operating point where V_{DS} and the power dissipation is zero. However, g_m has a dependency on the temperature, therefore it will be influenced by self-

heating. Changing the temperature modifies g_m mainly due to the temperature dependency of two other parameters that are the threshold voltage (V_T) and the mobility (μ) [7]. Since g_m is the first derivative of the drain current I_D, we can analyse its temperature dependence by observing the V_G-I_D curves for different temperatures (Fig. 6). At higher temperatures, V_T decreases. With a smaller V_T, the device turns on at a lower V_G, which means that for moderate-to strong inversion saturation, I_D would increase more quickly at higher temperatures; hence g_m would increase with temperature. On the other hand, μ gets smaller at larger temperatures. Therefore, once the device is turned on, the rate of change of I_D would be lower at higher temperatures. As a result of this, for devices in strong inversion and in saturation, g_m would increase with increasing temperature. Considering these two opposite trends, with the increasing temperature, g_m would be larger for lower V_G values and it starts to be smaller for higher V_G. Since the temperature increase due to device self-heating is more prominent for large V_G (strong inversion and saturation), we assume that self-heating decreases g_m inside the region of interest. Consequently, input referred thermal noise voltage increases according to (5) which worsens the noise figure of an amplifier.

Fig. 7 shows the input referred thermal noise voltage for the two cases where self-heating thermal model is active and inactive. It can be seen that under larger power dissipation, the difference between the two cases becomes also larger for the input referred noise voltage. For large V_{DS} values, the error can be more than 35%, which is twice larger than the error made in the thermal noise current. This is because g_m also drops with self-heating. Moreover, the optimum biasing point, where $S_{v,in}$ is minimum, shifts slightly down when self-heating is considered. Consequently, one might miscalculate the optimum bias point, if self-heating effect is not taken into account. It can also be observed that the noise increases as the device is deeper in saturation. Therefore, for having the lowest possible noise voltage, the devices should be biased closer to the linear region so that the undesired effects, like excessive self-heating, hot electrons, high velocity saturation and avalanche multiplication, are prevented as much as possible.

IV. Conclusion

In this paper, the thermal noise performance of MOSFET devices in 28nm FD-SOI technology is examined by considering their self-heating effects with a compact self-heating thermal model. It is shown that the thermal noise current (S_i) of short channel devices increases significantly with self-heating of the device. For large V_{DS} values, the increase can be around 18%. In addition to this, the input referred thermal noise voltage ($S_{n,in}$) also increases due to self-heating. Besides, the increase in $S_{n,in}$, which can go up to 37% at large V_{DS} values, is even more prominent than S_i mainly due to the drop in g_m at larger temperature values because of self-heating.

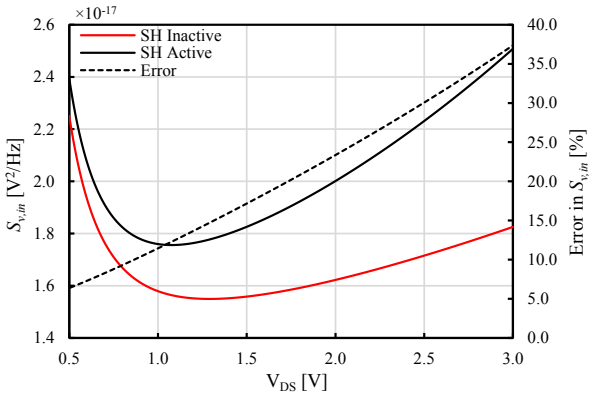

Fig. 7: Input referred thermal noise voltage ($S_{v,in}$) of 30nm device for self-heating thermal model active and inactive and the percentage of error.

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